RD53

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US ATLAS Upgrade Meeting

SLAC, July. 7, 2015

Outline

- Introduction
- Technical Progress in FY15
  - Preliminary <u>analog</u> design guidelines for radiation tolerance
  - Logic radiation tolerance
  - I/O and data compression
  - FE65-P2 Prototype
- Plans for FY16
  - FE65-P2
  - RD53A

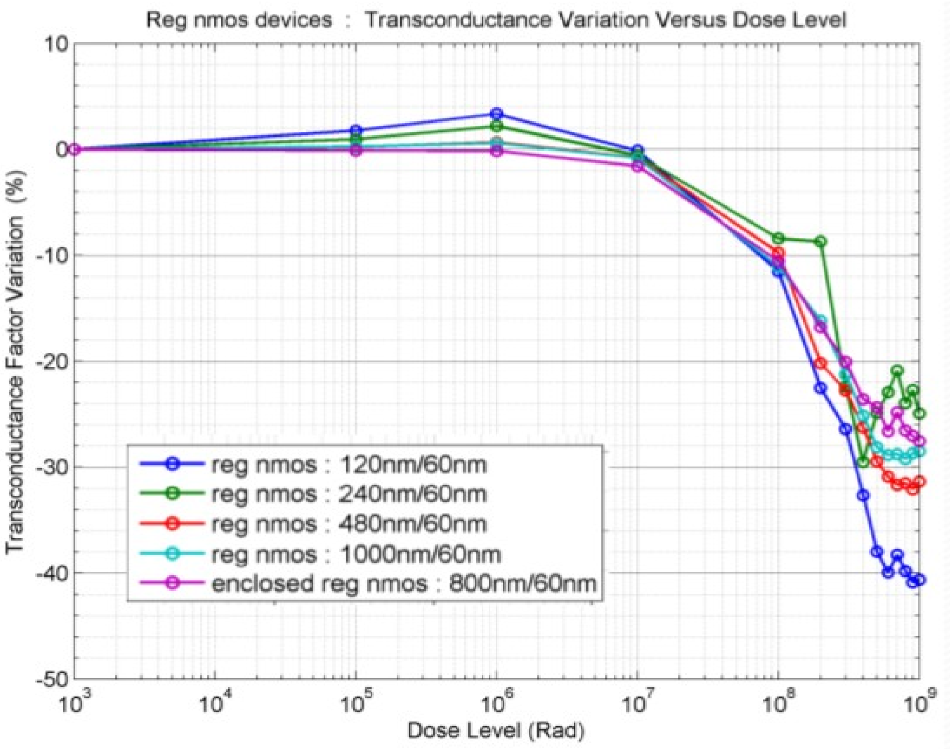
Introduction

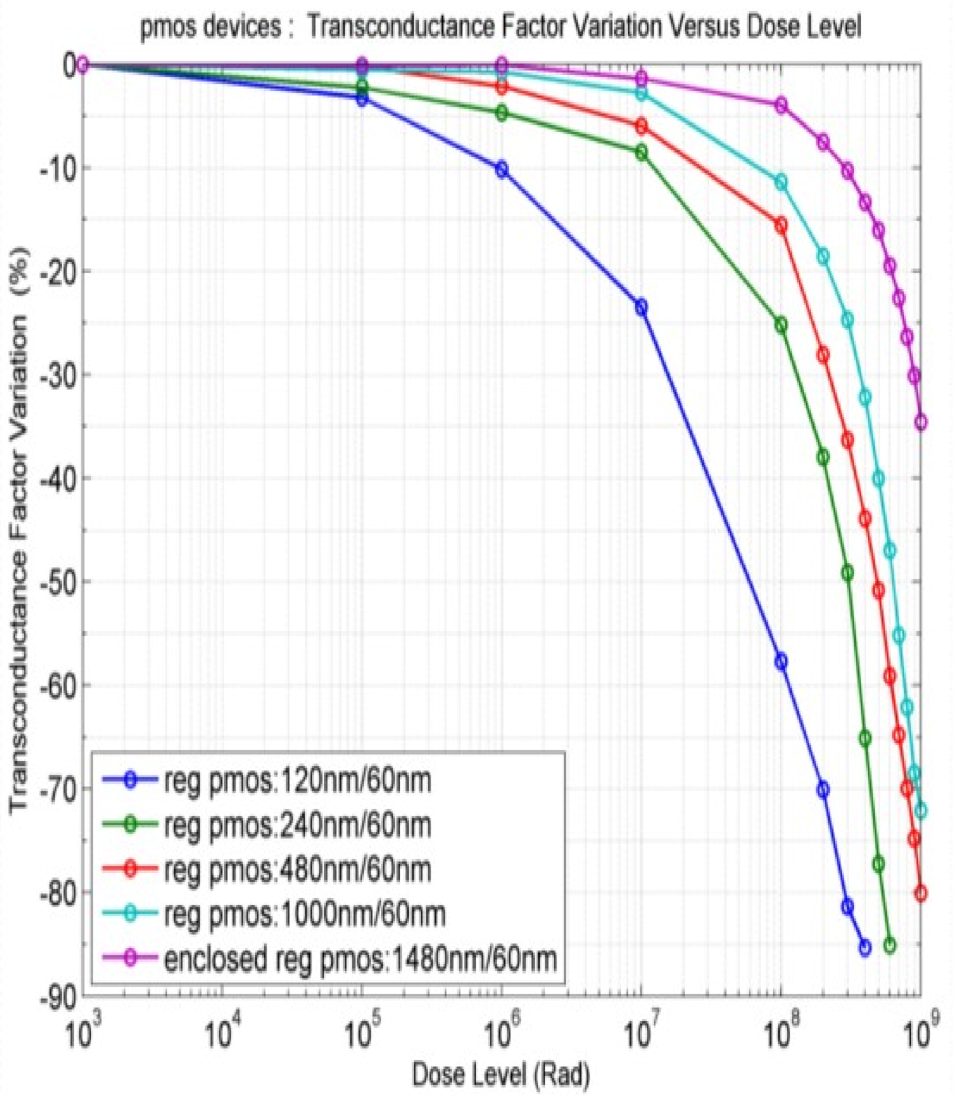
- RD53 has 20 member institutes
  - Web page: cern.ch/RD53
- US Institutes
  - LBNL, UCSC, UNM, Fermilab (CMS)
  - New bid join: OSU
  - Possible in near future: Penn

Radiation tolerance

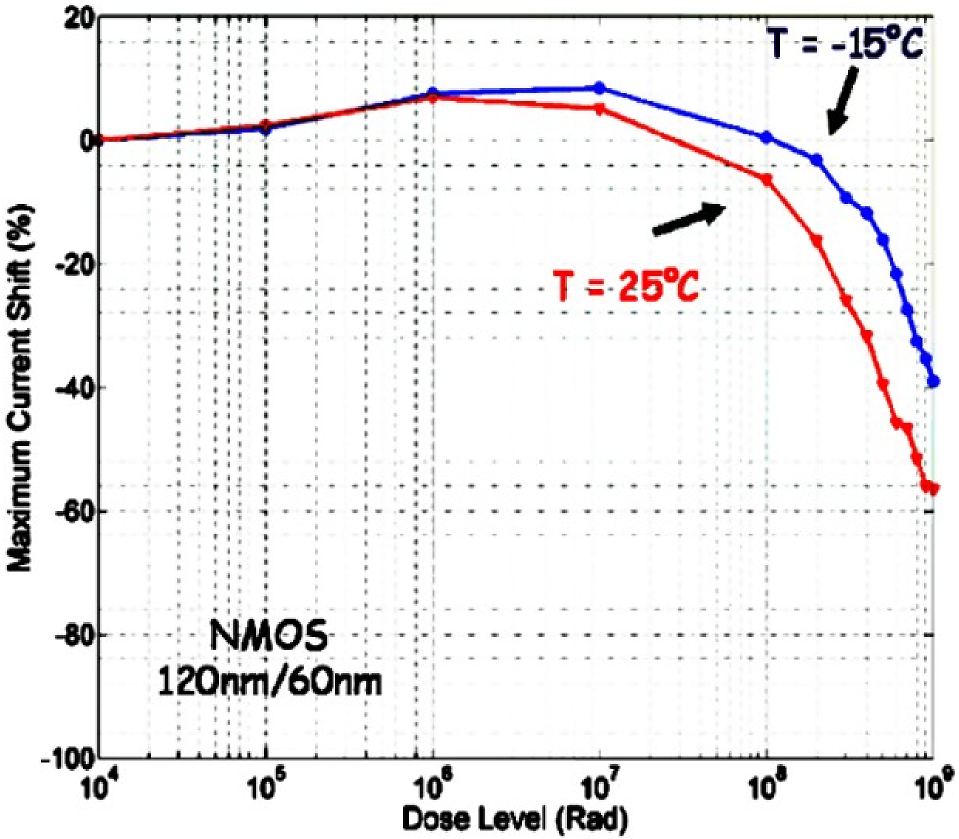
- Extensive investigations at the single transistor level
- --> Guidelines for analog design
- Guidelines currently given for 500Mrad only, not 1Grad
  - Guidelines will lead to good performance after 500Mrad
  - Design may also work up to 1Grad, but the amount of degradation between 500Mrad and 1Grad is very sensitive to details of bias conditions, temperature, and annealing
- Working on 500Mrad models for “corner” simulation.
- NMOS L>=120nm, any W.
- PMOS(#) L>=120nm (*), W>=300nm.
- (*) For most of the dose delivered at T <= -15C
- (#) With design simulation in 500Mrad corner

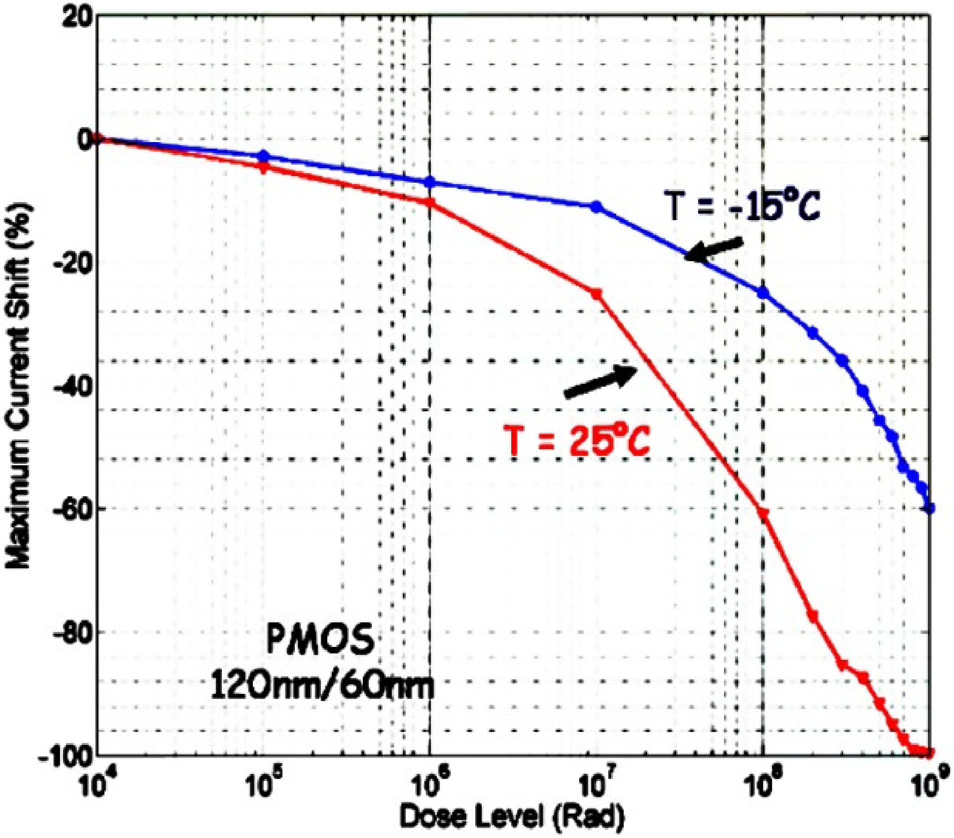
NMOS and PMOS of varying width





Minimum size at different temperature



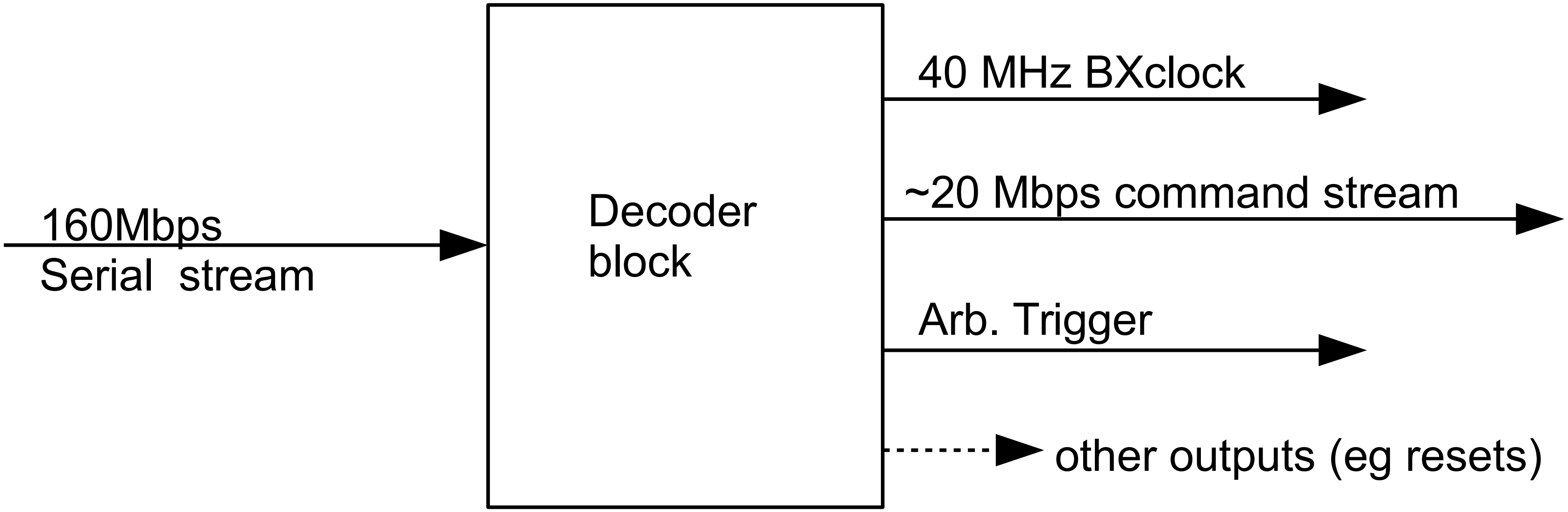


Logic Radiation Tolerance

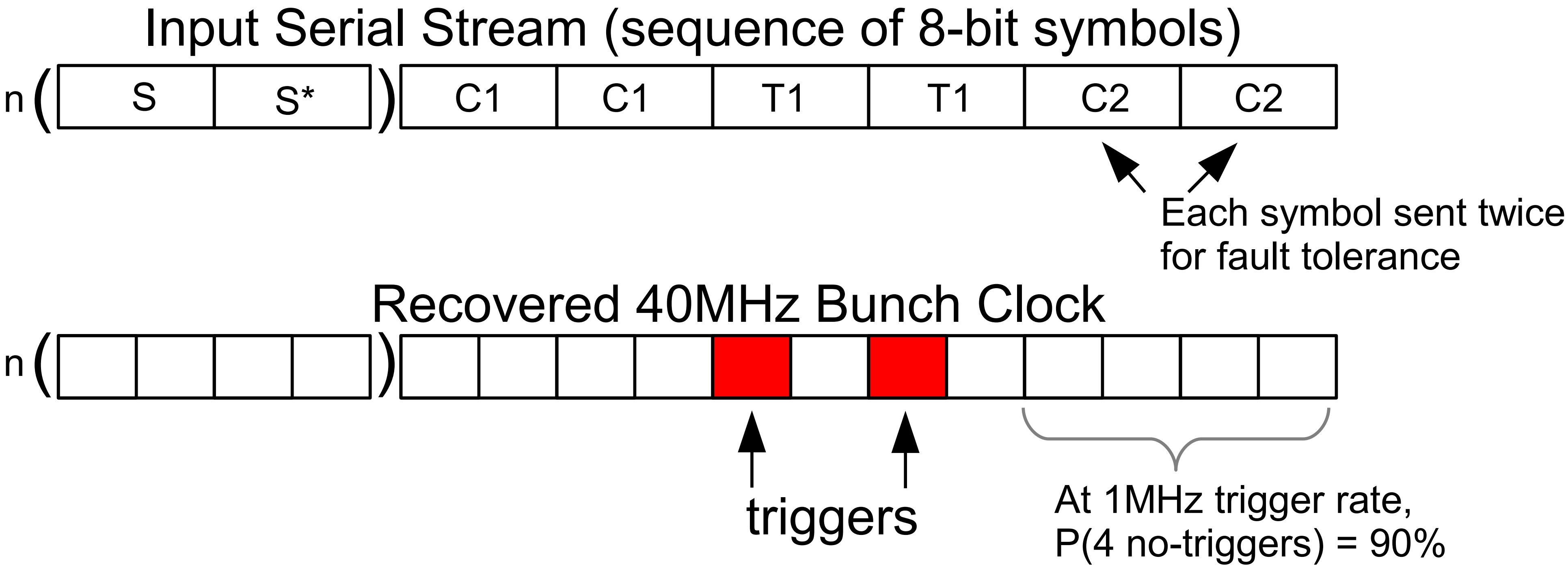
- Effect on logic standard cells must be evaluated
- Not clear whether choosing cells that respect analog guidelines is too conservative or not sufficient (or just right).
- Digital switching is less sensitive to gain than analog circuits
- But logic synthesis relies on knowing timing behavior of all cells (and corners)
- Work in progress. Synergy with characterization of logic libraries for cryogenic operation (DUNE) work being done at Penn.
- Discussions between Penn, NIKHEF, CPPM to use common test structures and characterization procedure for both radiation and low temperature.

Command/Control Protocol

- A single serial stream does it all
- DC balanced and allowing 40MHz clock recovery
- Can trigger on any arbitrary combination of beam crossings
- Commands always active (in parallel with triggers)
- Fault tolerant



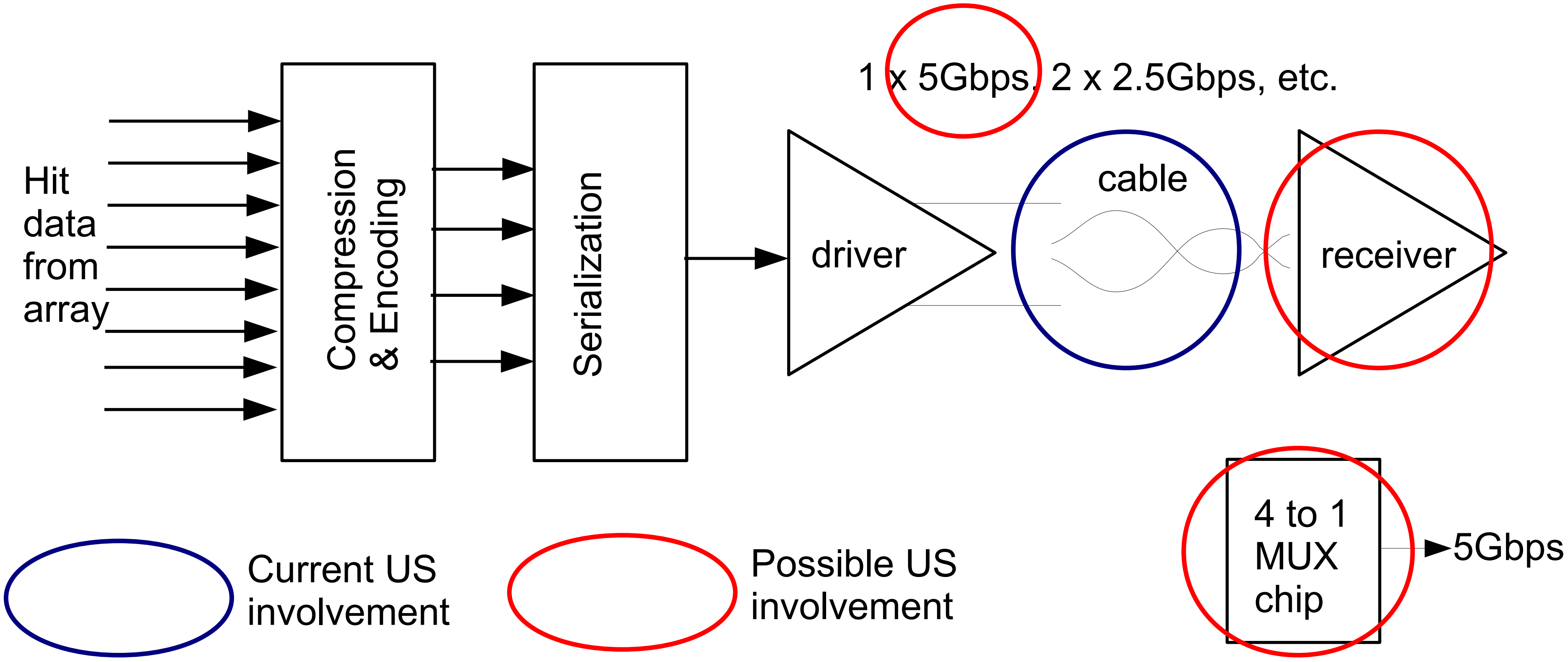
How it works



- S = synchronization symbol. Cannot occur accidentally and has transitions for clock recovery. Eg. 10000001
- C, T = command or trigger symbol. DC balanced, not ending or starting in 000 or 111. There are 54 such symbols. 15 used for T.
- No US design work on implementation

High speed output links

- Designed to drive electrical transmission lines 4 to 6m long
- RD53 taking a system approach to the data output design, not stopping at the chip pads
- Cable models are an important input from the experiments



65nm Test Chips

Chip name or n/a	Ready for submission date	Delivery date	Total area	contents
Proto65	June 2014	Sept. 2014	2 x 2 mm^2	Test devices, ADC, BG, Buffer, TSENS, SEU latches
Chipix65_1	Oct. 2014	Jan. 2015	3 times 2 x 2 mm^2	v1 Pixel Very Front Ends, Bandgap (INFN+CPPM), DAC, SRAM, Serdes. Hosting Prague DAC
FE65_P2	June/July 2015		7 to 15 mm^2	core layout demonstrator
Chipix65_2	May 2015	August 2015	2 times 2 x 2 mm^2	v2 Pixel Very Front Ends (2x 64-pixels-matrices), sLVDS RX/TX, D2RA digital cells, SerDEs, ADC. Including PonReset (Sevillia), SER from Bonn
Proto65_V2	May-June 2015		2 x 2 mm^2	IP blocks
DHPT1.1	~June 2015		12mm2	Belle2 production, C4 bumps, ~8-9 wafers extra
Chipix65_3	Autumn 2015	-	MPW ~12 mm^2 ?	t.b.d.
CLICpix, bis	End 2015 / early 2016		MPW ~13 mm2	CLIC-compatible pixel chip; 128*128 pixels

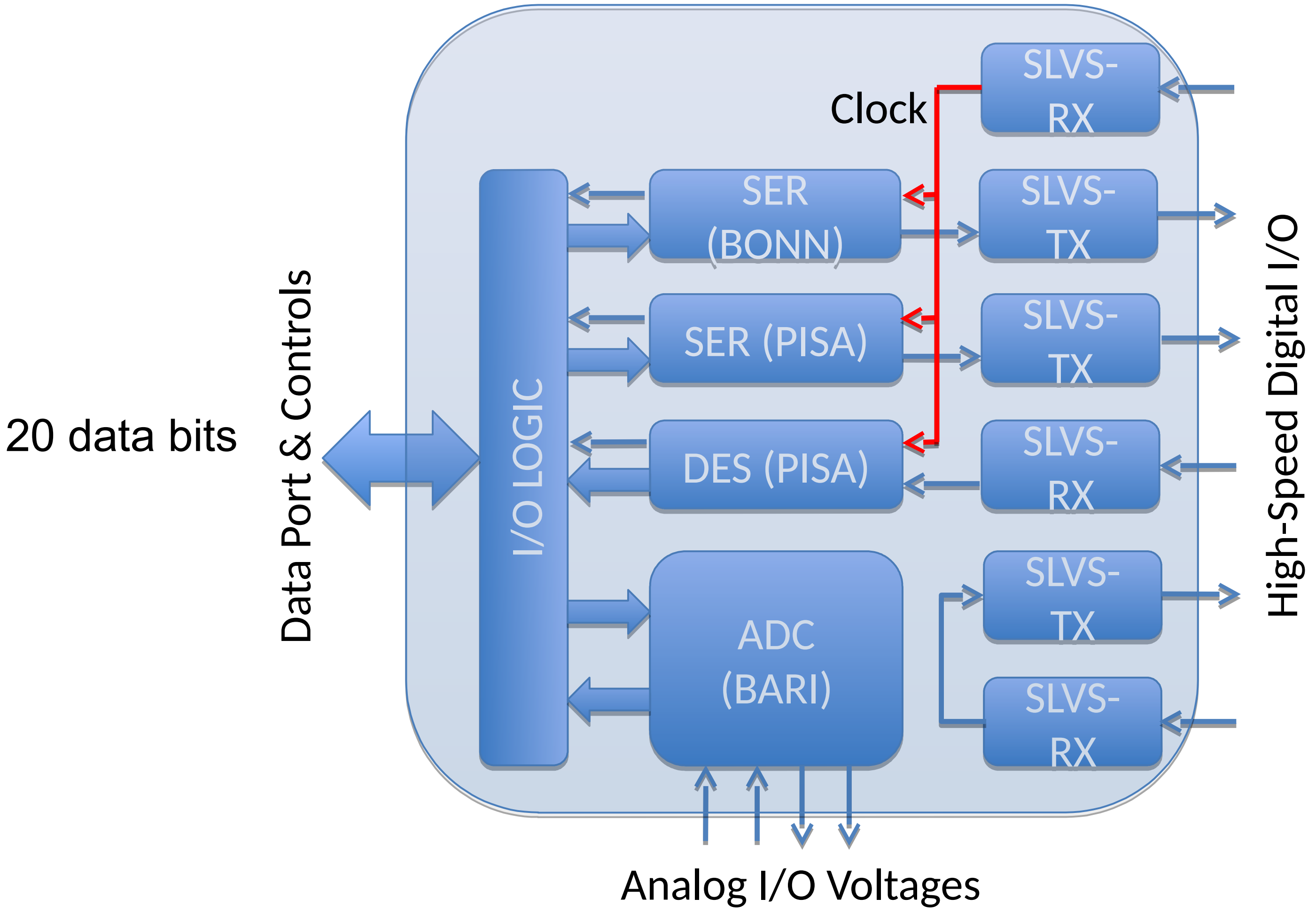
Analog IP Circuit Blocks

Name	Function	Status (march 2014)
TempSense	Temperature sensor	Proto
RadSense	Radiation sensor	Scematic
HvLeak	HV leakage current in pixel sensor	Schematic
AnalogBuf	Analog buffer for on/off-chip	Layout
BandGapBergamo	Band gap reference: DTNMOS	Proto
BandGapCppm	Band gap reference: Bipolar, DTMOS	Proto
BandGapCern	Band gap reference: Bipolar, DTNMOS	Proto
DacBari	12bit Current DAC	Proto
DacPrague	12bit Voltage DAC	Proto
AdcBari	12bit Wilkinson ADC	Schematic
AdcCppm	12bit SAR ADC	Proto
AdcCern	12bit Wilkinson ADC	Proto

PllSerDes	PLL, serializer, de-serializer, prog. delay	Layout/Proto
DiceLatch	SEU immune DICE latch	Proto
DiceMem	SEU immune DICE RAM	Proto
RadMem	Rad hard SRAM	Proto
LpClock	Low power clock driver/receiver	Schematic
RadIo	Rad hard IO with core transistors	Proto
SlvsDrvLS	Low speed SLVS driver	Proto
SlvsDrvHS	High speed SLVS cable driver	
SlvsRec	SLVS receiver	Proto
ShuntLdo	Shunt LDO for serial powering	Layout
PowerRes	Power on reset	Schematic

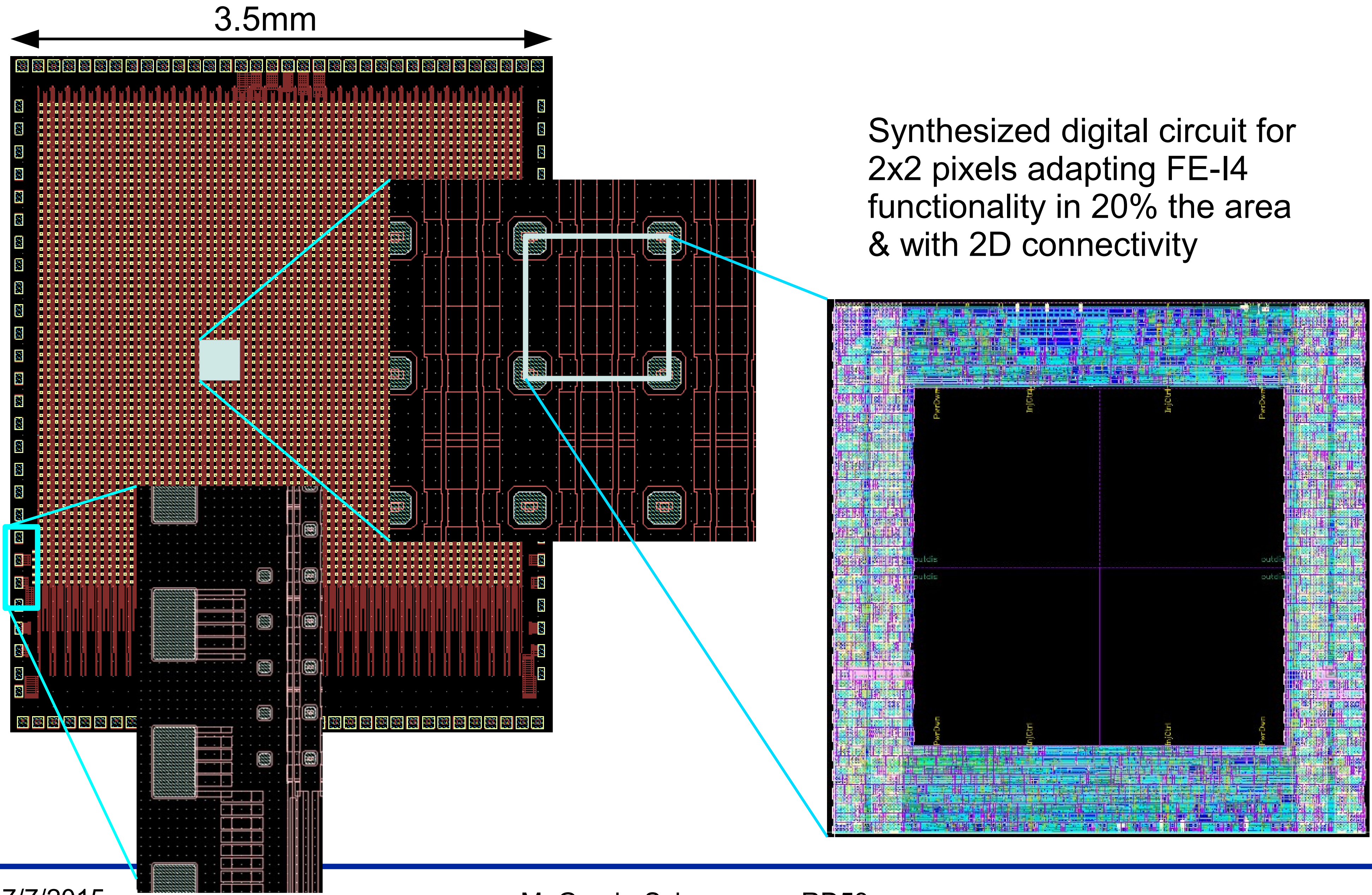
Bonn/Pisa/Bari SerDes

Version 2 just submitted (May 2015). 2mm x 2mm test chip



3.2 Mbps TX/RX (expected to be limited to somewhat less by test chip packaging)

FE65_P2 (LBNL & Bonn)



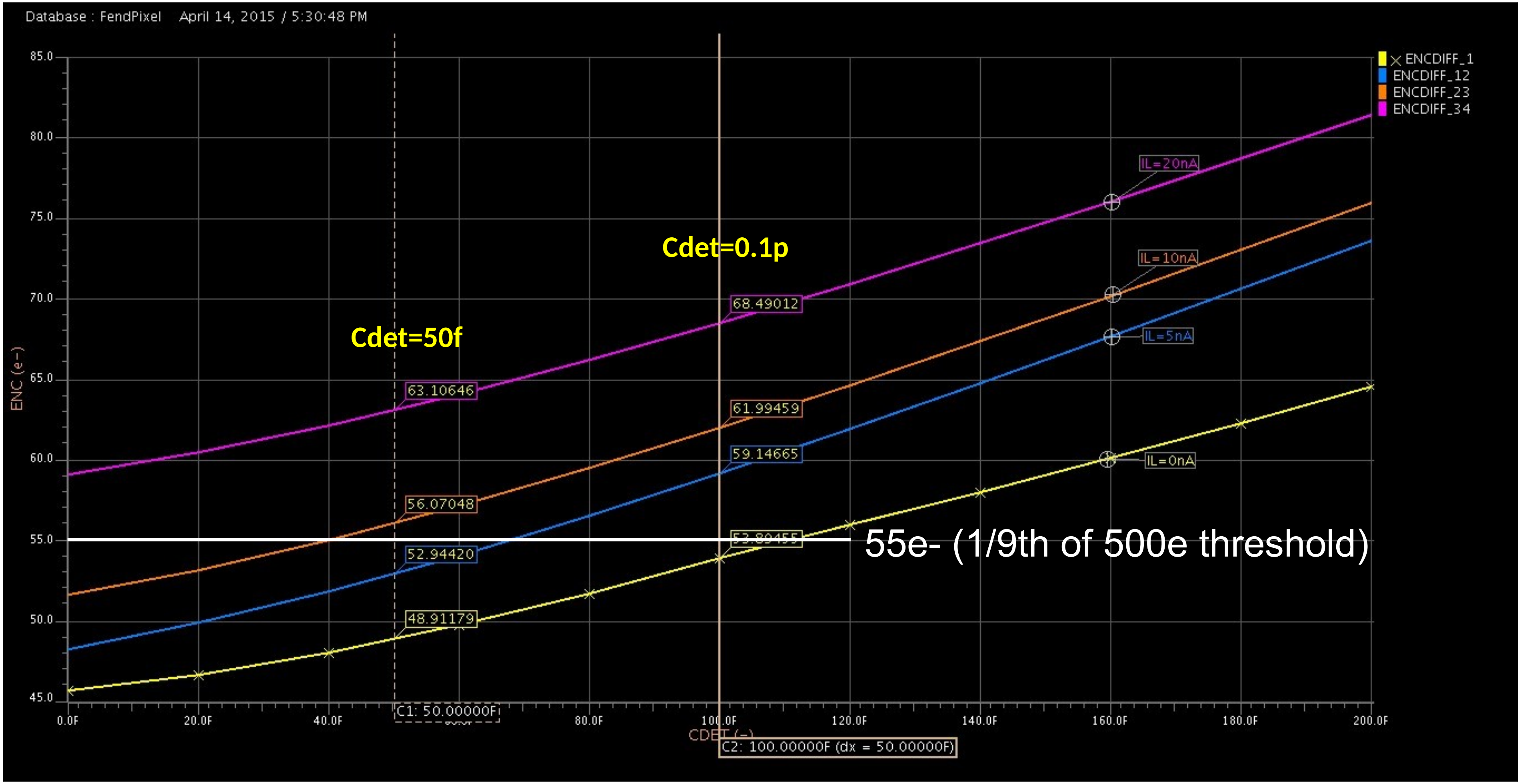
Synthesized digital circuit for 2x2 pixels adapting FE-I4 functionality in 20% the area & with 2D connectivity

FE65_P2 Goals

- Multi-project run submission now in August (delayed)
- Validate “analog islands in digital sea” layout giving 2D digital connectivity
- Validate analog / digital isolation strategy with digital top level design flow.
- Demonstrate low threshold stability (related to above)
  - This requires a bump bonded sensor
  - Planning single-chip to single-chip bump bonding (SLAC)
    - (tedious, low volume process, OK for above goals)
  - Matching 64 x 64 sensor prototypes included in upcoming sensor R&D runs (not part of RD53)

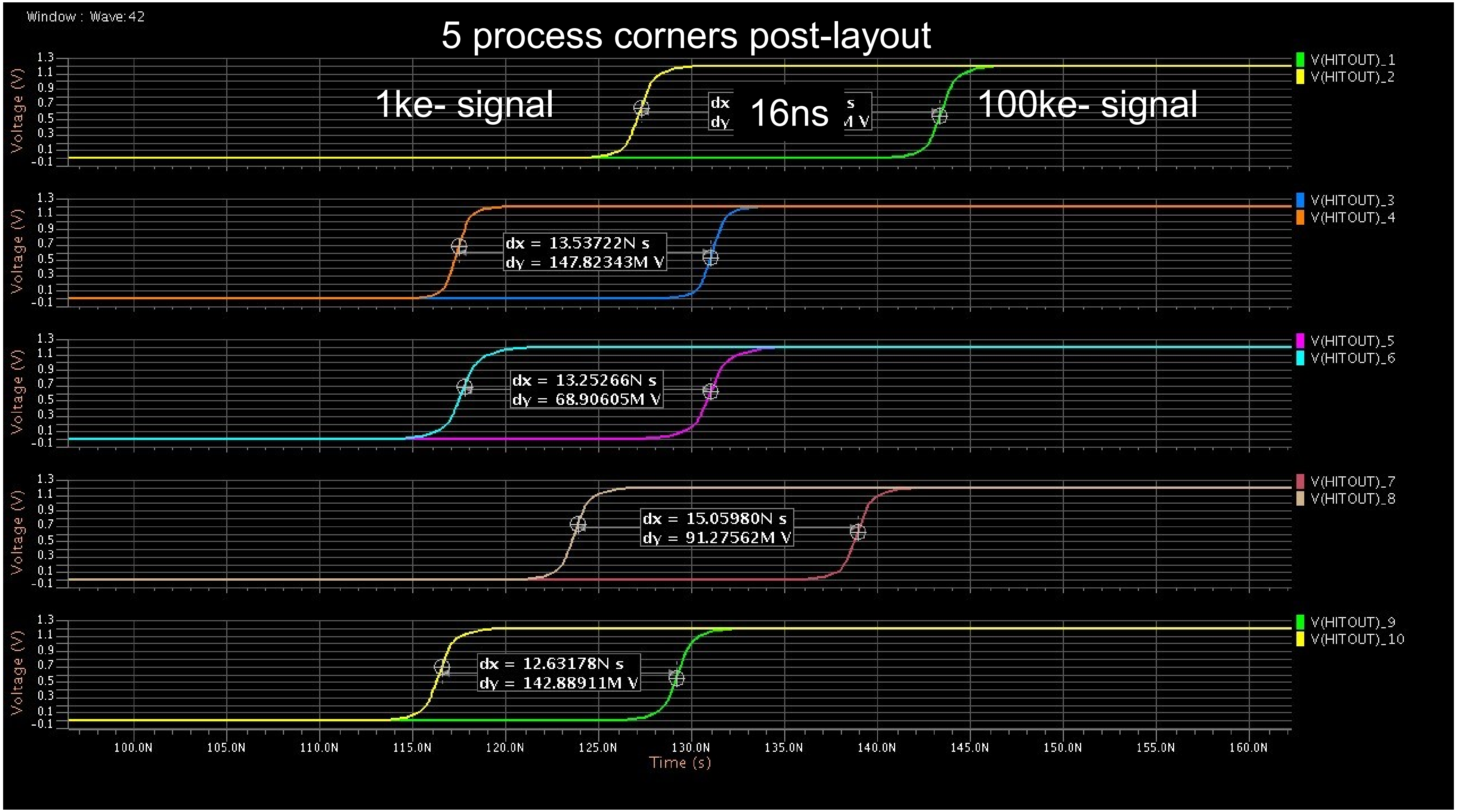
Analog performance example, noise

5uA/pixel power supply. **Noise vs. capacitance and leakage current**



Analog performance example, time walk

500e- discriminator threshold. 100fF and 5nA leakage. **5uA/pixel power supply**



FE64-P2 FY16 Plans

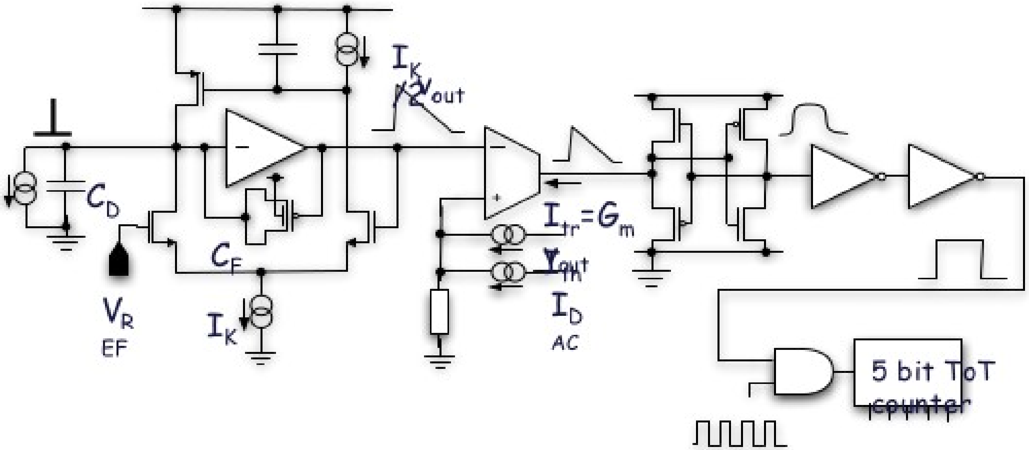
- Submit in August 2015
- Chips back in October
- Initial Bench tests in November / December
- First irradiation in December (to be checked with UNM)
- Produce first bump bonded assemblies also in December? (check with SLAC)
- Test irradiated parts in 2016
  - Likely need additional irradiation in 2016
- Test bump bonded assemblies in 2016
  - If they work well enough put in test beam

RD53A

- Large format chip in a full wafer engineering run
- Demonstration of essential features
  - high rate, low threshold, high speed readout
  - 500Mrad radiation tolerance (to be tested also at higher dose)
  - SEU tolerance
  - Power management, serial power
  - Yield
- Not a production chip
  - Multiple pixel variants (non-uniform array)
  - Not ultimate performance data output drivers, data compression not required, minimal bells and whistles, high volume test features, etc
  - Necessary for RD53 <u>and</u> for sensor and bump bonding R&D efforts

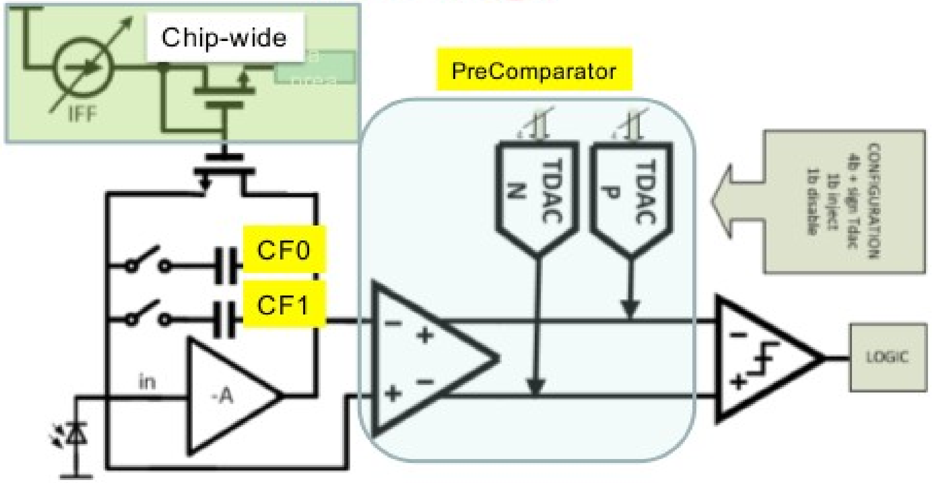
Analog Variants (evolving)

INFN-Pavia design



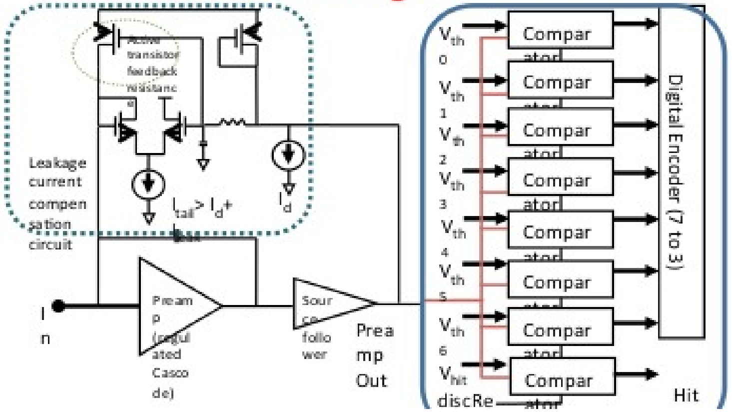
Single stage with current comparator and ToT counter

LBNL design



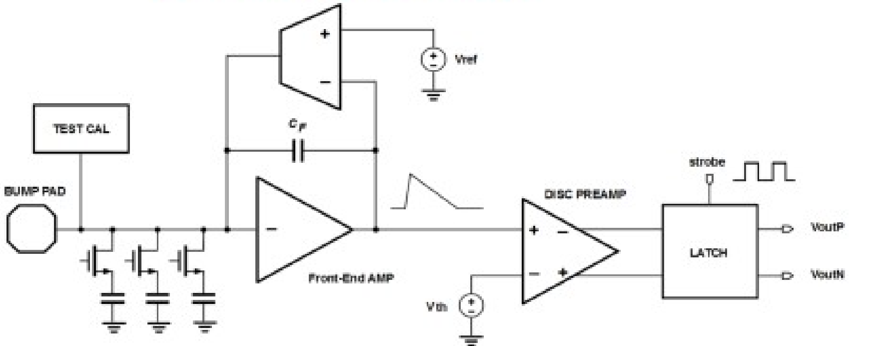
1 of 4 in quad “analog island” of FE65_P2

FNAL design



Synchronous: resets every bunch crossing. Flash ADC

INFN-Torino design



Single stage with SAR-like ToT counter using synchronous comparator

RD53A schedule

- Currently finalizing draft specs document within RD53
- Circulate to ATLAS and CMS for comment in July
- Freeze and approve ahead of RD53 October meeting
- Start full chip integration end of 2015
  - First design review Jan or Feb 2016
- Submit chip in 2016, but not yet clear when yet
  - Need resource loaded work plan
  - Aiming for a joint submission with CMS MPA to make it affordable

RD53A Specs

CERN-RD53-NOTE-15-00x

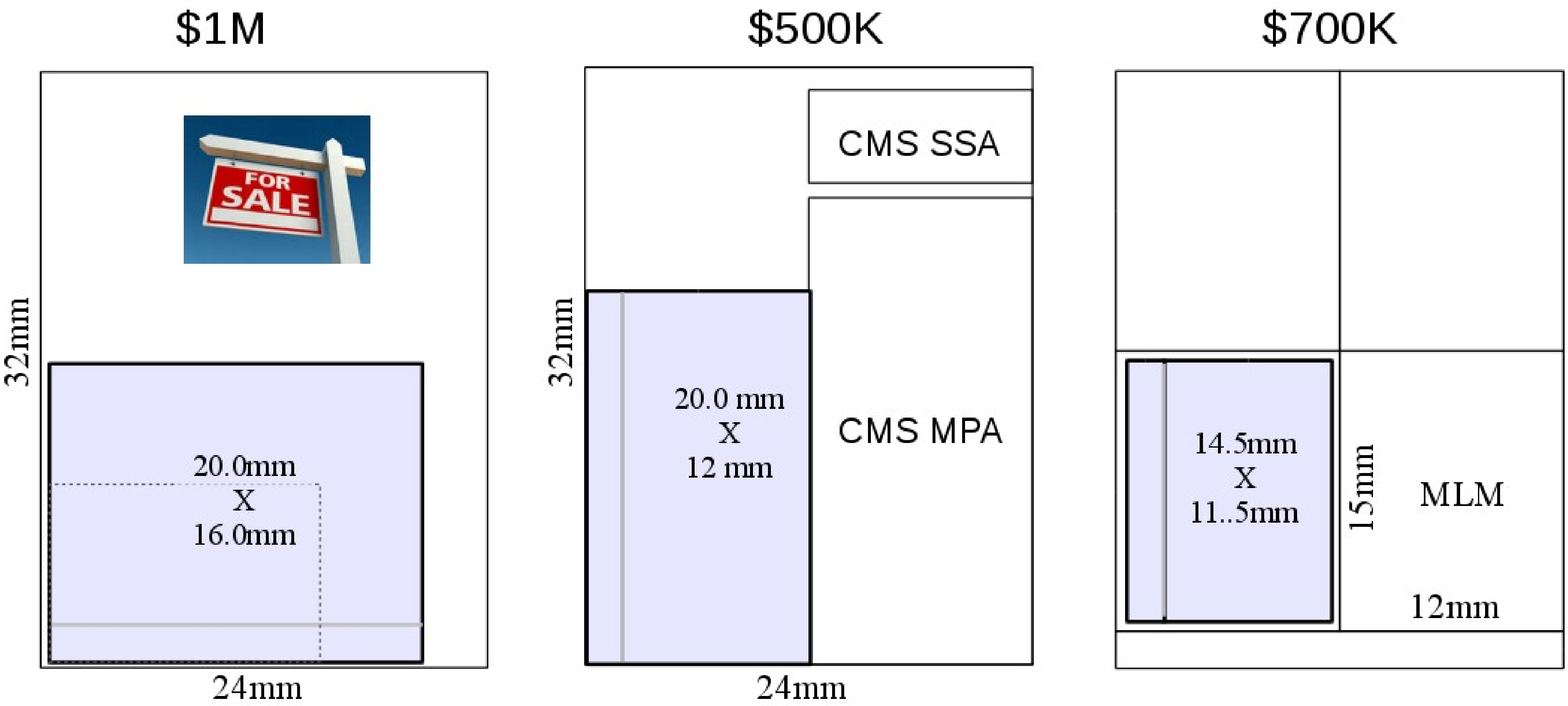
Version 0, June 7, 2015

RD53A Integrated Circuit Specifications

ABSTRACT: Specifications for the RD53 collaboration's first wafer scale inte
for hybrid pixel detector readout, called RD53A. RD53A is intended to dem
format IC the suitability of the technology (including radiation tolerance), the s
operation, and the high hit and trigger rate capabilities, required for HL-LHC u
and CMS. The wafer scale production will permit the experiments to protot
assembly with prototype sensors in this technology and to measure the perf
assemblies. RD53A is not intended to be a final production IC for use in an ex
contain design variations for testing purposes, making the pixel matrix non-unif

Contents

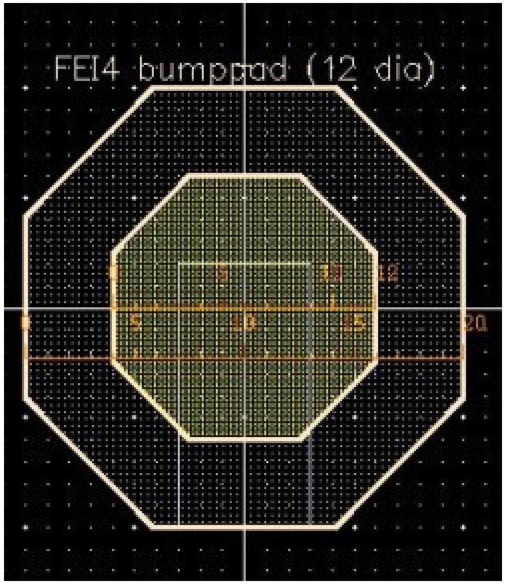
Size options

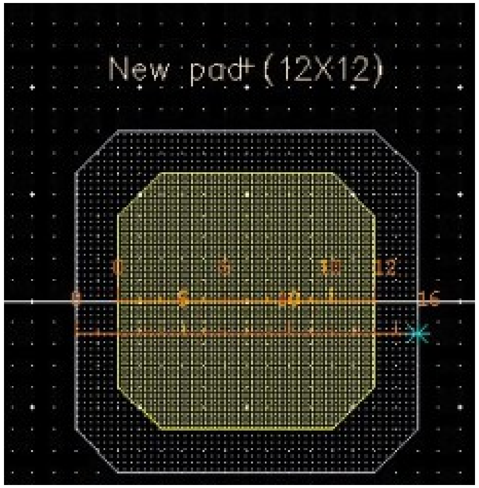


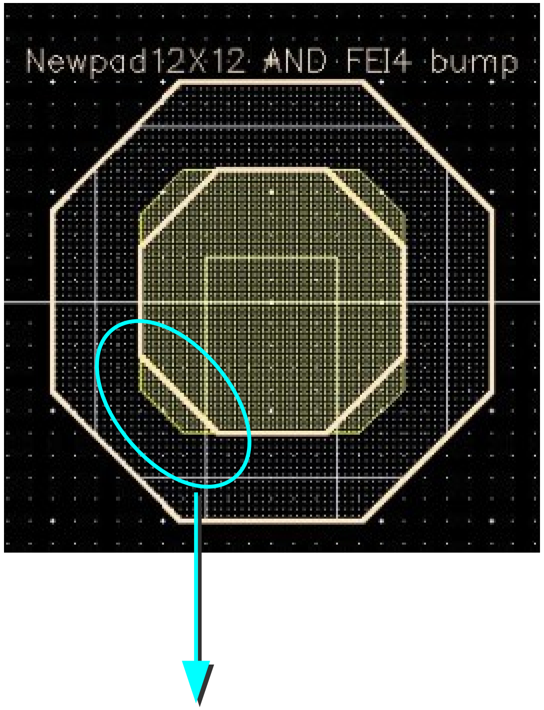
BACKUP

FE65_P2 Bump Pad

Shape must be different than FE-I4 (different layout rules)





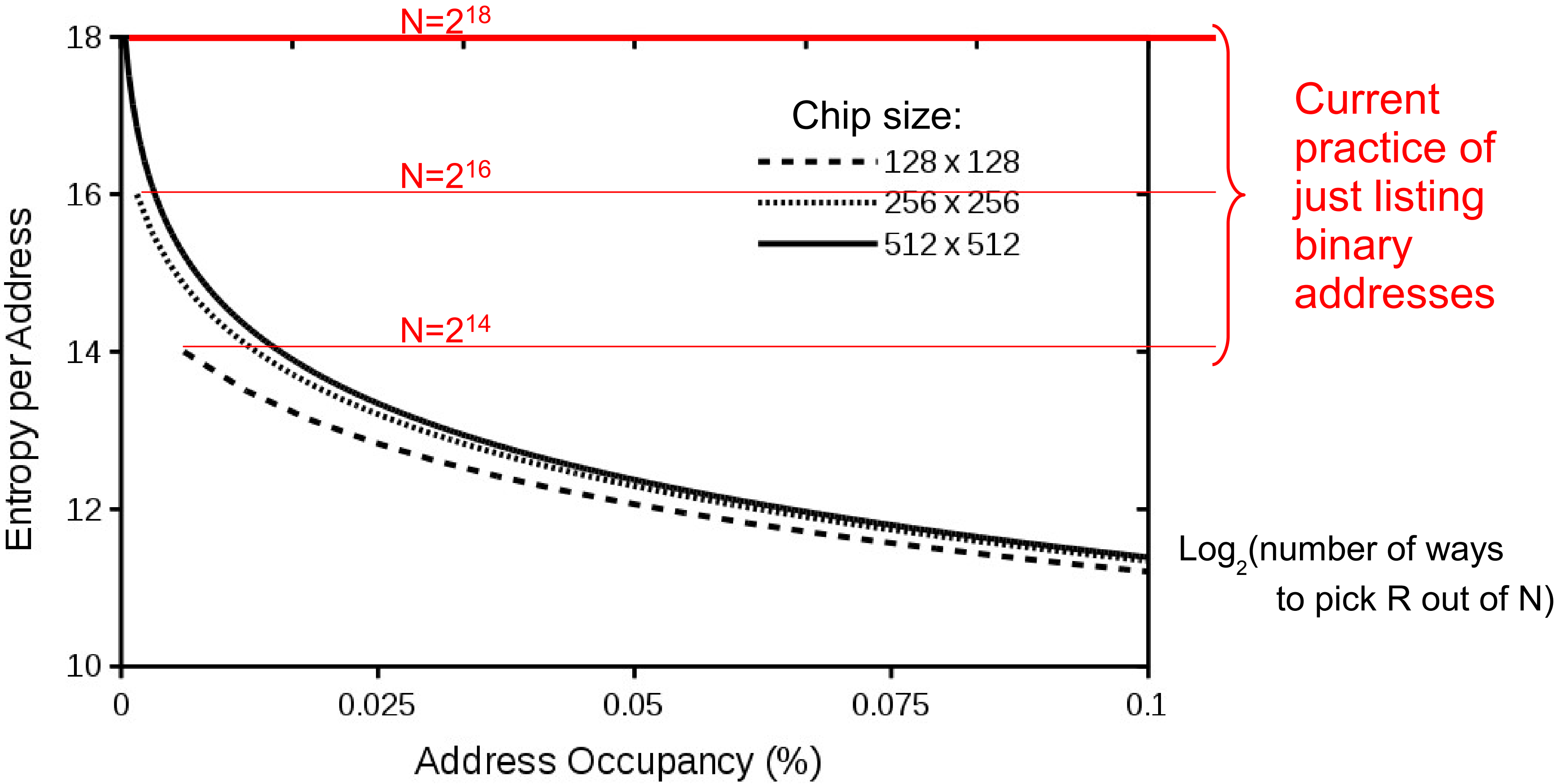


Less metal
(lower capacitance,
higher density)

Slightly bigger opening

Information, not bits

- Example of information entropy in pixel or cluster addresses



- For details see books.google.com and search "data compression efficiency in silicon detector readout"

Edge pixels

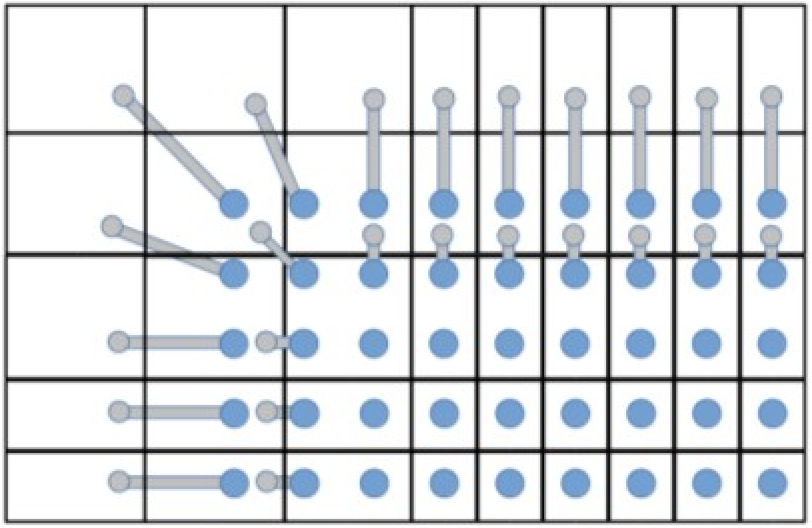
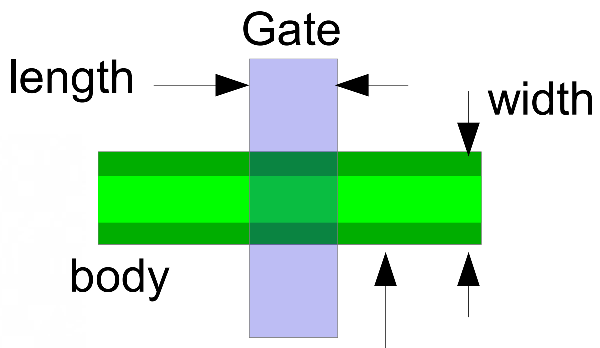


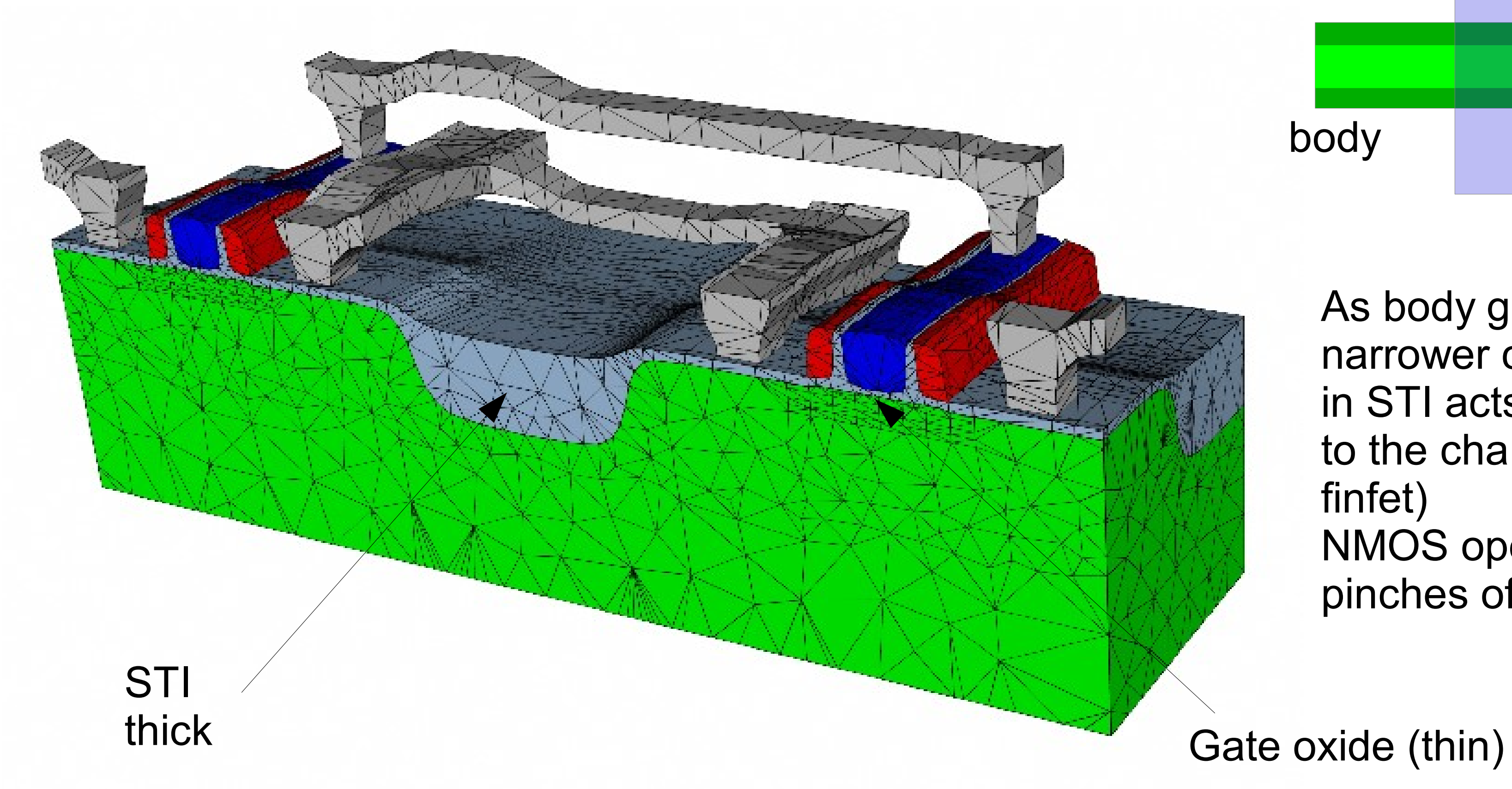
Figure 3: Diagram showing pixels in an abuttable corner of an example sensor, making use of the RD53A special edge pixels to cover inter-chip gaps. Sensor pixel boundaries and one-layer sensor metal are shown. The larger blue circles are on a $50 \times 50\mu m^2$ grid matching the RD53A bump pad locations. 12 Normal pixels ($50 \times 50\mu m^2$) can be seen at the bottom right of the figure. The remaining sensor pixels are larger, together creating 150 μm of gap coverage, without any need for crossed metal routing.

Effect of STI charge buildup (RINCE)

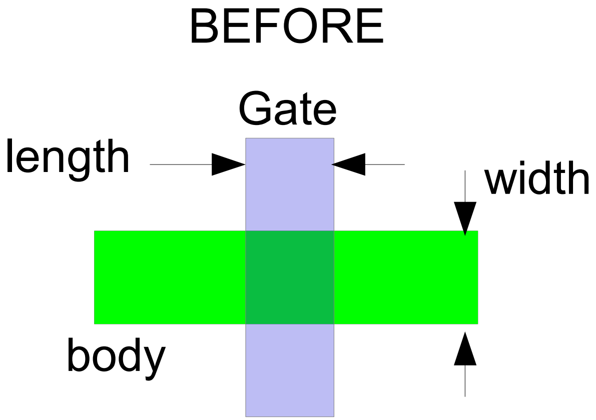
F.Faccio and G.Cervelli, IEEE TRANS. NUCL. SCI, VOL. 52, NO. 6, 2005

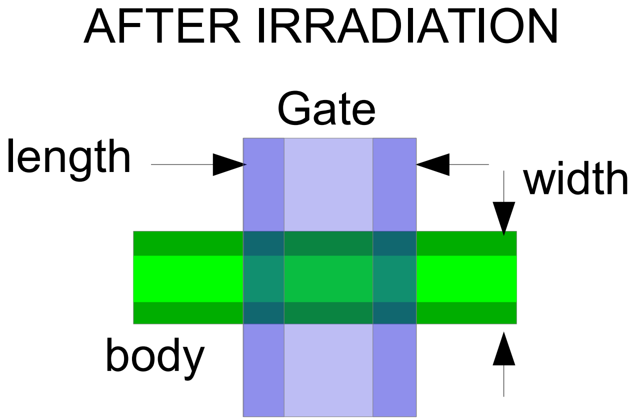


As body get narrower and narrower charge trapped in STI acts as “side gates” to the channel (a parasitic finfet)
NMOS opens up, PMOS pinches off.



+ A previously unobserved length effect



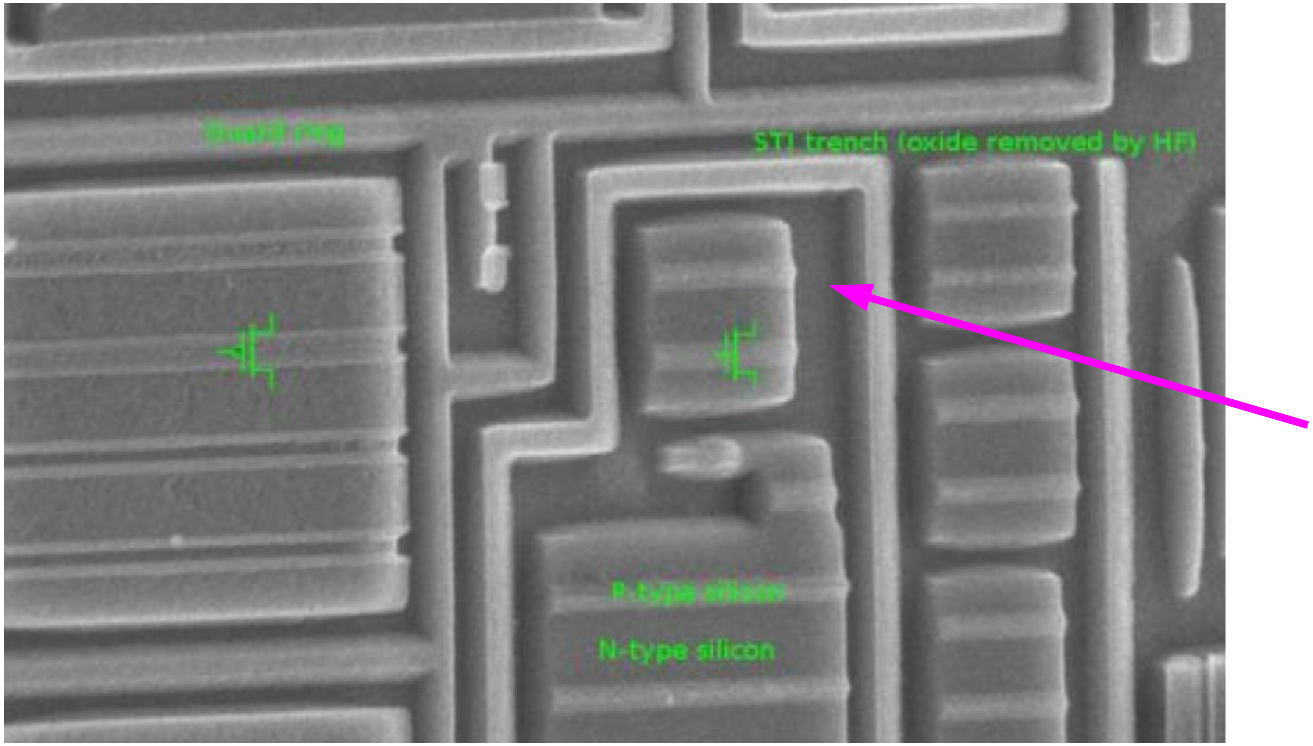


Obviously not a physical lengthening of the channel
Behaves as if this happens

- Length mechanism characterized empirically but device physics not understood
- Both small width and small length get hit- not good news for min. Size devices.
- (Same effects are there in 130nm, but can't make small enough transistors to clearly see them)

Width effect has a known damage mechanism

- **Small feature size CMOS technology is radiation hard because the gate oxide is leaky due to QM tunneling. This prevents charge build-up in the gate oxide**
- **But there are other oxides that are not thin enough for QM tunneling, and charge trapping in them eventually matters.**



These trenches are normally full of oxide called STI (shallow trench isolation)